UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,181	06/02/2006	Wojtek Sudol	US030477US2	2881

24737 7590 05/22/2008
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
DOUGHERTY, THOMAS M	

ART UNIT	PAPER NUMBER
2834	

MAIL DATE	DELIVERY MODE
05/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,181	SUDOL, WOJTEK	
	Examiner	Art Unit	
	Thomas M. Dougherty	2834	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 4/15/08 have been fully considered but they are not persuasive. Erickson et al. teach the advantage of having a thin IC, which teaching is employed by the Applicants.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 8, 12, 15, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erikson et al. (2003/0018267). Erikson et al. show (fig. 5) an ultrasound transducer probe, comprising: an attenuation backing substrate (23); an integrated circuit (32) coupled to the attenuation backing substrate (23), wherein the integrated circuit (32) is translucent to acoustic waves (see paragraph [0048]); and an array of piezoelectric elements (18) coupled to the integrated circuit (32); the array of piezoelectric elements (18) having an acoustic matching layer (30, see claim 7) disposed on a first surface of the array thereof.

The integrated circuit (32) includes a thickness sufficiently small for causing the integrated circuit to be translucent to acoustic waves. See paragraph [0047].

The thickness of the integrated circuit (32) is on the order of approximately 50 μm.

See paragraphs [0047] and [0049] in which it is noted that the thickness aspect of the integrated circuit is the same as that of the silicon layer.

The array of piezoelectric elements (18) includes a one-dimensional array (as shown).

Erikson shows a method of fabricating an ultrasound transducer probe, comprising: providing an attenuation backing substrate (23); coupling an integrated circuit (32) to the attenuation backing substrate (23), wherein the integrated circuit (23) is translucent to acoustic waves, as noted above; and coupling an array of piezoelectric elements (18) to the integrated circuit (32); the array of piezoelectric elements (18) having an acoustic matching layer (30) disposed on a first surface of the array (18) thereof.

The integrated circuit (23) includes a thickness sufficiently small for causing the integrated circuit (23) to be translucent to acoustic waves, as noted above.

The thickness of the integrated circuit (23) is on the order of approximately 50 μm, as noted above.

The array of piezoelectric elements (18) includes a one-dimensional array, as noted above.

Erikson et al. do not specifically state that the thickness of the integrated circuit is less than 50 μm.

Erikson et al. clearly teach the desirability and advantage of having an acoustically translucent IC and the achievement of such by making the component thin. Therefore it would have been obvious to one of ordinary skill in the art to achieve even

greater acoustic translucence by having the IC component thinner than 50 μm. Thinness in this instance is a result effective variable. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide for an IC component in the device of the Applicants' invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Claims 2, 9, 11, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erikson et al. (2003/0018267). Given the invention of Erikson et al. as noted above, they do not note the attenuation allowed by their backing material. Note however that the applicants do not disclose in these claims what material is employed.

It would have been obvious to one having ordinary skill in the art to employ an attenuation backing substrate includes a material capable of providing an attenuation on the order of approximately 10 dB/cm at 5 MHz to 50 dB/cm at 5 MHz since it has been held to be within the skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Claims 3, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erikson et al. (2003/0018267) further in view of Odaka et al. (JP 06-090950). Given the invention of Erikson et al. as noted above, they do not show an ultrasonic transducer array which *inter alia* has an attenuation backing substrate that includes

epoxy composite materials that consist of epoxy and a mixture of very high and very low acoustic impedance particles.

Odaka et al. note a backing member for an ultrasonic probe that has areas of low and high impedance. He doesn't note his specific material.

It would have been obvious to one having ordinary skill in the art to have high and low impedance sections in the backing of an ultrasonic probe device in order to better focus the beam, as is taught by Odaka et al. in their PURPOSE. Regarding the material or materials chosen for such a backing, it has been held to be within the skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erikson et al. (2003/0018267) further in view of Ossmann (US 2006/0150380). Given the invention of Erikson et al. as noted above, they do not show note that their integrated circuit includes at least one of a silicon based, a gallium based, and a germanium based integrated circuit or an integrated circuit that solely includes a silicon based integrated circuit.

Ossmann shows (fig. 2) and notes (paragraph [0085]) a silicon base integrated circuit (110) for use in an ultrasound probe array assembly.

Ossmann does not note that the integrated circuit is translucent to acoustic waves.

It would have been obvious to use a silicon base integrated circuit in the device or Erikson et al. at the time of their invention, such as is clearly taught by Ossmann,

since the properties of silicon based integrated circuits are well known and thus have a predictable operation.

Additionally, it would have been obvious to one having ordinary skill in the art to use any of a silicon, gallium or germanium based intergrated circuit since these are all well known materials for integrated circuit construction and since it has been held to be within the skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erikson et al. (2003/0018267) further in view of Pattanayak et al. (US 5,655,276). Given the invention of Erikson et al. as noted above, they do not show a two-dimensional array.

Pattanayak et al. note that an ultrasound array can either be one or two dimensional for similar applications and that either arrangement is typical. See col. 1, lines 15-20.

Pattanayak et al. do not note a specific integrated circuit, or a backing with low and high impedance particles.

It would have been obvious to one having ordinary skill in the art to form the Erikson et al. invention into a two-dimensional array since such is noted as typical and since both one and two-dimensional arrays may serve similar purposes as Pattanayak et al. note.

Additionally, it would have been obvious to one having ordinary skill in the art to make the Erikson et al. array into a two-dimensional array, *mutatis mutandis*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direct inquiry to Examiner Dougherty at (571) 272-2022.

/T. M. D./ /Thomas M. Dougherty/

tmd Primary Examiner, Art Unit 2834

May 20, 2008